REMARKS

Request for Continued Examination

Applicant respectfully requests continued examination of the above-indicated application as per 37 CFR 1.114.

Claims 1-9 are rejected under 35 USC 103a as being unpatentable over Fujii et al US Patent No: 5,898,695 [herein after Fujii] and further in view of Ling et al, US Patent No: 6,732,255 [herein after Ling].

Concerning the independent claim 1:

Applicant has amended claim 1 to include the limitations that the host chip is engaged in controlling operations of the multi-chip system and the slave chip is engaged in executing servo control or signal detection. No new matter is entered. In particular, see paragraph [0004] of the original specification as filed.

Applicant asserts that the amendments to claim 1 should render claim 1 allowable over Fujii and Ling as neither Fujii nor Ling teach such operation. For example, Fujii teaches a slave unit being element 141 "Transit Buffer" and Ling teaches a slave unit being buffer memory being the slave unit (see Ling, Col 7. lines 1-11). Applicant notes that both transit buffers and buffer memories are not equivalent to a slave chip engaged in executing servo control or signal detection. Specifically buffers neither execute servo control nor execute signal detection. For at least this reason, applicant asserts that currently amended claim 1 should be found allowable over the cited references. Claims 2-21 are dependent upon claim 1 and should be found allowable for at least the same reason.

Additionally, further comments regarding the patentability of particular dependent claims is provided below.

Concerning the dependent claims:

Applicant notes that in the Office action mailed 02/07/2007, the Examiner appears to have not considered several of the applicant's previous arguments. Said arguments are further explained in the following, and applicant respectfully requests that the Examiner

consider these arguments as the current rejections of claims 2, 13, and 14 do not appear to be valid.

Firstly, concerning claim 2, applicant points out that none of the cited references, alone or in combination, teach the following limitation:
"wherein in step (b) the host chip further delivers a clock signal to the slave chip." (claim 2 – emphasis added)

In the rejection of original claim 2 by the Examiner in the Office action mailed 08/24/2006 and then repeated verbatim in 02/07/2007, the Examiner stated that the limitation "wherein the host chip further delivers a clock signal to the slave chip" is taught by Fujii in Fig.5, element 4. However, inspection of Fig.5 shows that the micro-processor 12 (interpreted by the Examiner as the host) does not deliver a clock signal to the transfer buffer 141 (interpreted by the Examiner as the slave). In particular, clock generator 4 does not generate a clock signal that is delivered to the slave chip. Instead, the clock generator 4 is shown generating a clock signal that is delivered to the microprocessor 12, which was interpreted as the host by the Examiner in the Office action of 08/24/2006.

In the Office action of 02/07/2007 the Examiner stated "it should be obvious to the Applicant that the host chip is combination of the above three mentioned elements" [Microprocessor (12), RAM (7) and Clock Generator (4)] Applicant notes that such an interpretation does not address the applicant's argument of the host chip not delivering the clock signal to the slave chip.

Fig.5 shows there are in fact two clock signals taught by Fujii and shown in Fig.5 that are delivered to the transfer buffer 141; however, applicant points out that neither is delivered by the microprocessor 12. Col 6, lines 49-54 only state, "The transfer buffer 141 is a buffer for outputting a TS packet onto a data bus, and transfers the data at high speed to RAM 7 through direct memory access (DNA), by performing data bit conversion and time axis conversion from transport path clock tsClock into data bus clock busClock." Applicant notes that the transport path clock is delivered by the transport path, and Fujii does not teach from where the busClock is delivered. Therefore, applicant asserts that claim 2 should not be found as being unpatentable over Fujii and further in view of Ling for at least the reason that neither reference teaches the "host chip is for delivering a clock

signal to the slave chip", as is claimed in claim 2. Reconsideration of claim 2 is respectfully requested.

Concerning claim 13, applicant points out that none of the cited references, alone or in combination, teach the following limitation:

"wherein in step (b), when being informed by the slave chip, the host chip further for delivering a clock signal to the slave chip, and when not being informed by the slave chip, the host chip not delivering the clock signal to the slave chip." (claim 13)

In the Office action of 02/07/2007, the Examiner stated that Fujii, col. 4, lines 44-50 teach said limitation. However, inspection of col. 4, lines 44-50 states only the following with respect to the clock signal, "The apparatus may further comprises: means for generating a clock signal in accordance with clock information in the encoded stream". Applicant points out that Fujii simply does not teach or suggest that the host chip is for delivering a clock signal to the slave chip when being informed by the slave chip, and for not delivering the clock signal to the slave chip when not being informed by the slave chip, as is claimed in claim 13 of the present invention. Fujii only mentions that a clock signal may be generated in accordance with clock information in the encoded stream. Examples of encoded streams are shown in Figures 19,20, and 24 by Fujii.

Applicant notes that none of the figures by Fujii or anywhere else in the teachings of Fujii does he mention when the host is to deliver the clock signal to the slave device and when the host is not to deliver the clock signal to the slave device. However, applicant has specifically claimed such functionality in claim 13 of the present invention. In order to be rejected under 25 USC 103, each and every limitation of claim 13 should be found taught or suggested by at least one of the cited references (or their combination), and for at least this reason applicant asserts that claim 13 should not be found rejected in view of the cited references of Fujii and Ling. In short, neither Fujii nor Ling teach the limitations of claim 13 of when the host chip should and should not deliver the clock signal to the slave chip. Reconsideration of claim 13 is respectfully requested.

Finally, concerning claim 14, applicant points out that none of the cited references,

alone or in combination, teach the following limitation:

wherein in step (b) the host chip further delivering the clock signal to the slave chip having a predetermined number of clock cycles.

The Examiner stated in the Office action of 02/07/2007 that said limitation is taught by Fujii in col 8, lines 57-60. However, inspection of col 8, lines 57-60 states "The microprocessor 12 supplies a frequency acceleration/deceleration control signal to the clock generator 4. Generated clocks count up the timer 123. In this manner, a feedback loop is formed."

Applicant points out that accelerating and decelerating a clock signal is not equivalent to having a predetermined number of clock cycles. Neither Fujii nor Ling teach anything about clock cycles in general and therefore also do not teach that the clock signal has a predetermined number of clock cycles. Applicant also notes that continuous clock cycles (regardless of accelerated frequency or decelerated frequency) generated by the clock generator 4 should not be interpreted as a predetermined number of clock cycles because continuous (i.e., infinite) clock cycles is not equivalent to a predetermined number of clock cycles. For example, in the present invention (see paragraph [0022]), there are exactly thirteen clock cycles generated. Thirteen is a predetermined number and corresponds to the number of servo signals to be transferred. Applicant sees no similar limiting of the clock cycles with the teachings of Fujii and Ling to a predetermined number. The Examiner has cited a paragraph that also does not teach or suggest this limitation of the present invention as claimed in claim 14. For at least this reason applicant asserts that claim 14 should not be found rejected in view of the cited references of Fujii and Ling. Reconsideration of claim 13 is respectfully requested.

New Claims

Applicant has added new claims 21-28. Specifically, claims 21-28 claim a multi-chip system and correspond directly to limitations disclosed in paragraph [0022] and illustrated in Figures 1 and 3 of the original specification as filed. No new matter is entered.

Concerning the patentability of the new claims 21-28, applicant points out that neither Fujii nor Ling, either alone or in combination, teach or suggest the claimed

limitations. For example, as explained above for the amendment to claim 1, neither Fujii nor Ling teach a slave chip for executing servo control or signal detection, as is claimed in new independent claim 21. For at least this reason alone, applicant asserts that independent claim 21 and its dependent claims 22-28 should be found allowable with respect to the cited references. Consideration of the new claims 21-28 is respectfully requested.

Conclusion:

Thus, all pending claims are submitted to be in condition for allowance with respect to the cited art for at least the reasons presented above. The Examiner is encouraged to telephone the undersigned if there are informalities that can be resolved in a phone conversation, or if the Examiner has any ideas or suggestions for further advancing the prosecution of this case.

Sincerely yours,

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Note: Please leave a message in my voice mail if you need to talk to me. (The time in D.C. is 12 hours behind the Taiwan time, i.e. 9 AM in D.C. = 9 PM in Taiwan.)